Amendment to the Specification:

Please amend paragraphs 2 and 3 on page 8 of the specification, as follows:

In addition to the above, memory bus adapters may be used to couple one system to another system. This coupling is also performed using a multichannel link 118, such as an STI link. In one example, the STI link used to couple the systems is adapted to be used as an Integrated Cluster Bus (i.e., as a channel), as described in ~~U.S. Patent Application No. 09/151,117~~ U.S. Patent No. 6,442,613, entitled "Controlling The Flow Of Information Between Senders And Receivers Across Links Being Used As Channels", Gregg et al., ~~filed September 10, 1998~~ issued August 27, 2003, which is hereby incorporated herein by reference in its entirety.

Additional details regarding STI links are described in such references as U.S. Patent 5,757,297, entitled "Method and Apparatus for Recovering a Serial Data Stream Using a Local Clock", Ferraiolo et al., issued May 26, 1998; ~~U.S. Patent Application No. 08/660,648~~ U.S. Patent No. 5,859,881, entitled "Adaptive Filtering Method and Apparatus to Compensate For a Frequency Difference Between Two Clock Sources", Ferraiolo et al., ~~filed on June 7, 1996~~ issued January 12, 1999; U.S. Patent No. 5,522,088, entitled "Shared Channel Subsystem Has A Self Timed Interface Using A Received Clock Signal To Individually Phase Align Bits Received From A Parallel Bus", Halma et al., issued May 28, 1996; U.S. Patent No. 5,651,033, entitled "Inter-System Data Communication Channel Comprised Of Parallel Electrical Conductors That Simulates The Performance Of A Bit Serial Optical Communications Link", Gregg et al., issued July 22, 1997; and U.S. Patent No. 5,787,094, entitled "Test And Diagnostics For A Self-Timed Parallel Interface", Cecchi et al., issued July 28, 1998, each of which is hereby incorporated herein by reference in its entirety.